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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/475,879	12/30/99	LACEY	T 0325.00292

EXAMINER	
TRAN, A	
ART UNIT	**PAPER NUMBER**
2819	

021363 MM91/0308
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DATE MAILED: 03/08/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application N .	Applicant(s)	
	09/475,879	LACEY ET AL.	
	Examiner	Art Unit	
	Anh Q. Tran	2819	

-- The MAILING DATE of this communication appears on the cover sh et with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 December 1999* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15) ☒ Notice of References Cited (PTO-892)
16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
17) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4* .
18) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
19) ☐ Notice of Informal Patent Application (PTO-152)
20) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-2, 6-7, & 10-15 are rejected under 35 U.S.C. 102(b) as being anticipated by Cliff et al (5,689,195).

Regarding claim 1, Cliff shows a programmable logic device (Fig. 1) comprising:

One or more horizontal routing channels (60 & 70);

One or more vertical routing channels (80);

One or more logic elements each configured to connect between one of the horizontal routing channels and one of the vertical routing channels, wherein the logic element comprises a logic block array (horizontal blocks 30 to the left of memory block 40) and a memory block (40).

Regarding claim 2, Cliff shows the memory block is connected to one of the horizontal (connect to 60 through MUX 454) and one of the vertical routing channels (connect to 80 through buffer 452).

Regarding claim 6, Cliff shows the memory block is placed within the logic block array (Fig. 1).

Regarding claim 7, Cliff shows a plurality of I/O blocks, wherein each I/O block of the plurality of I/O blocks is connected to a different end of the horizontal (140) and the vertical routing channels (160).

Regarding claim 10, Cliff shows one or more dedicated inputs for I/O cell control (180, Fig. 4).

Regarding claim 11, Cliff shows one or more dedicated clocks inputs (200, Fig. 4).

Regarding claim 13, Cliff shows the dedicated inputs for I/O control comprise a reset input (662, Fig. 9).

Regarding claim 14, Cliff shows the dedicated inputs for I/O control comprise an output enable input (692, Fig. 9).

Regarding claim 15, Cliff shows the dedicated inputs for I/O control comprise an output enable input (180).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 3-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cliff '195 in view of Veenstra (5,977,791).

Cliff shows the claimed invention except for the memory block is configured as a synchronous dual port memory or as an asynchronous dual port memory or as a synchronous FIFO.

However, in figures 7-9 of Veenstra shows the memory block is configured as an synchronous dual port memory or as an asynchronous dual port memory or as a synchronous FIFO.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the memory block (Fig. 7-9) of Veenstra in place of the memory block of Cliff (40) in order to enhanced the logic functions.

5. Claims 12 & 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cliff'195 in view of Jefferson et al (6,130,552).

Cliff shows the claimed invention except for a phase lock loop circuit configured to generate one or more global clock signals in response to one or more input clock signals.

However, Jefferson shows a phase lock loop circuit (Fig. 5 & 6) configured to generate one or more global clock signals (GCLK) in response to one (300) or more input clock signals.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide a phase lock loop circuit (Fig. 5 & 6) of Jefferson in the programmable logic device in order to reduces or minimizes clock skew when distributing a clock signal within the integrated circuit.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Young (5,933,023) and Agrawal et al (6,181,163 B1) disclose a programmable logic device comprises array of logic blocks and RAM blocks.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh Q. Tran whose telephone number is 703-306-4507. The examiner can normally be reached on M-F (8:00-5:30) second Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Tokar can be reached on 703-305-3493. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7724 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Anh Tran
February 26, 2001

Michael J. Tokar

Michael Tokar
Supervisory Patent Examiner
Technology Center 2800